



Pathways for 1000× Energy Efficiency

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CEA-Leti, Deputy Director and CTO

July 1st, 2025





1. Context

Who are we?

FROM HARDWARE TO SOFTWARE - A GLOBAL R&D PARTNER ADDRESSING SEMICONDUCTOR CHALLENGES



- 2,000 scientists & engineers
- € 500M budget
- 3,400 patents
- 11,700 m² cleanrooms
- 700 tools
- 78 startups
- 700 publications / year

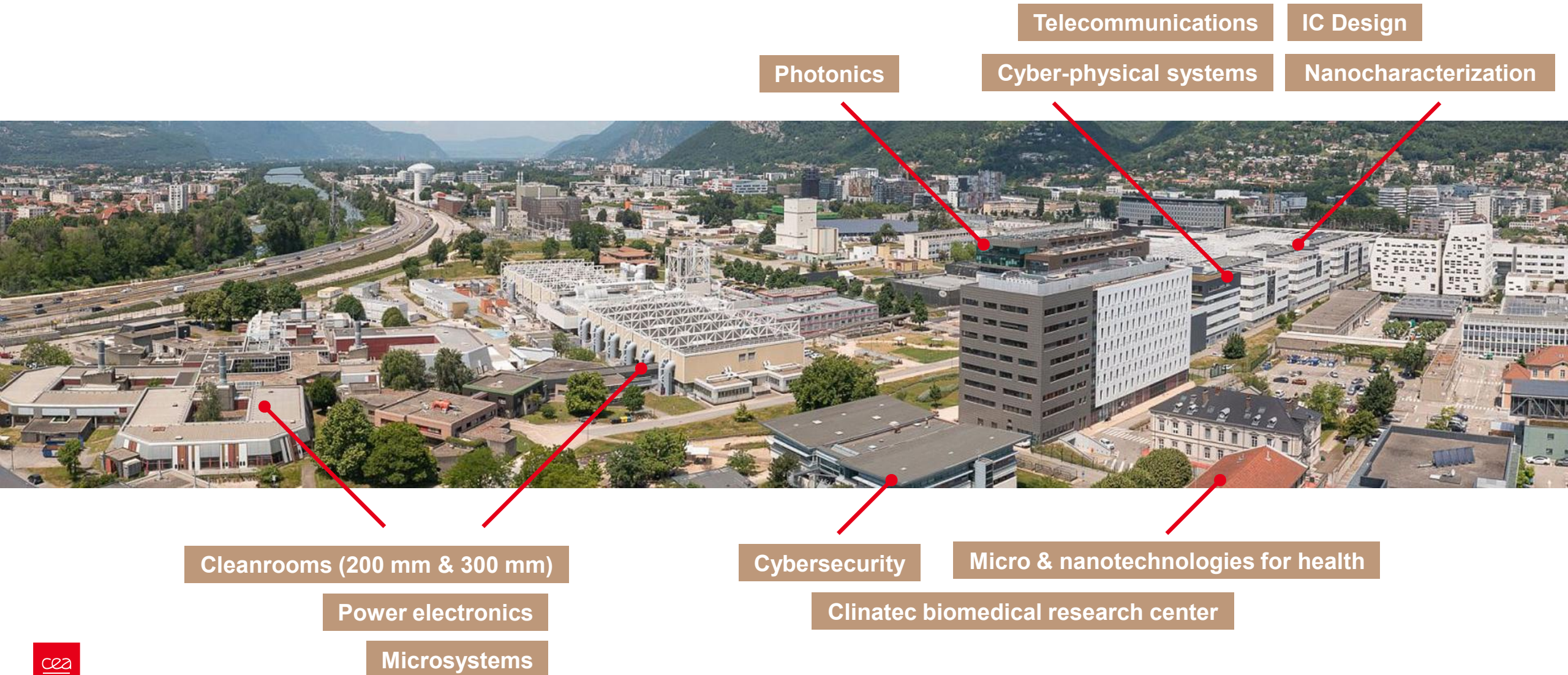


- 1,000 scientists & engineers
- € 130M budget
- 700 patents
- 26 startups
- 300 publications / year



- We collaborate with semiconductor players in industry and research organizations
- To meet societal and market challenges via bilateral projects
- Anticipating electronic trends with a global vision and R&D programs
- Leveraging state of the art semiconductor technologies and tools, and a lab-to-fab approach

A WIDE RANGE OF WORLD-CLASS R&D FACILITIES ON A SINGLE CAMPUS





WE NEED A DIGITAL WORLD THAT IS **COMPETITIVE, SECURE, ETHICAL, AND SUSTAINABLE,** IN LINE WITH OUR VALUES



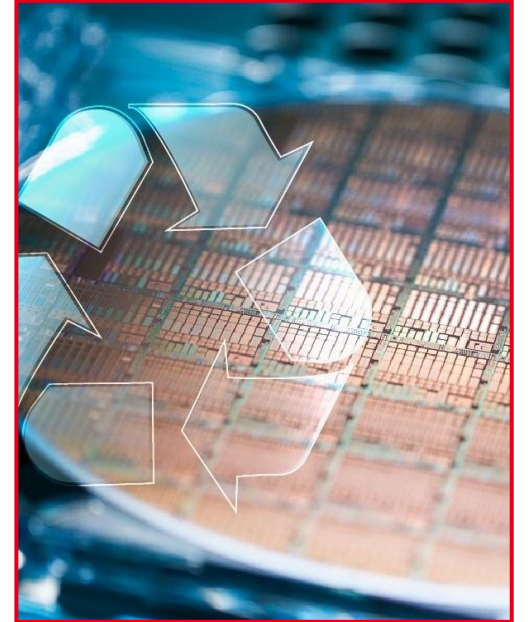
COMPETITIVE
(performance & cost)



SECURE



ETHICAL



SUSTAINABLE

AS SOCIETY'S DIGITALIZATION ACCELERATES, BREAKTHROUGH INNOVATIONS ARE NEEDED

Major challenges to address:

- Energy efficiency
- Sustainable electronics

Breakthrough innovations are required:

- in semiconductor technologies
- in circuits and chip architectures
- in systems, algorithms, and EDA tools



**We need to improve
the energy efficiency
of chips and
electronic systems
by a factor of 1,000
by 2032**

CONTEXT

1

Data Deluge & Energy Demand

The irreversible trend.

A DATA-DRIVEN ERA

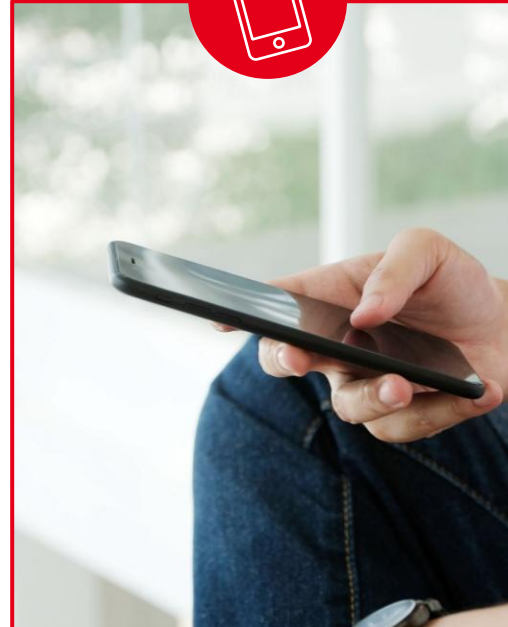
2024 GLOBAL FIGURES



World population
8.2 billion



Internet users
5.35 billion (60%)



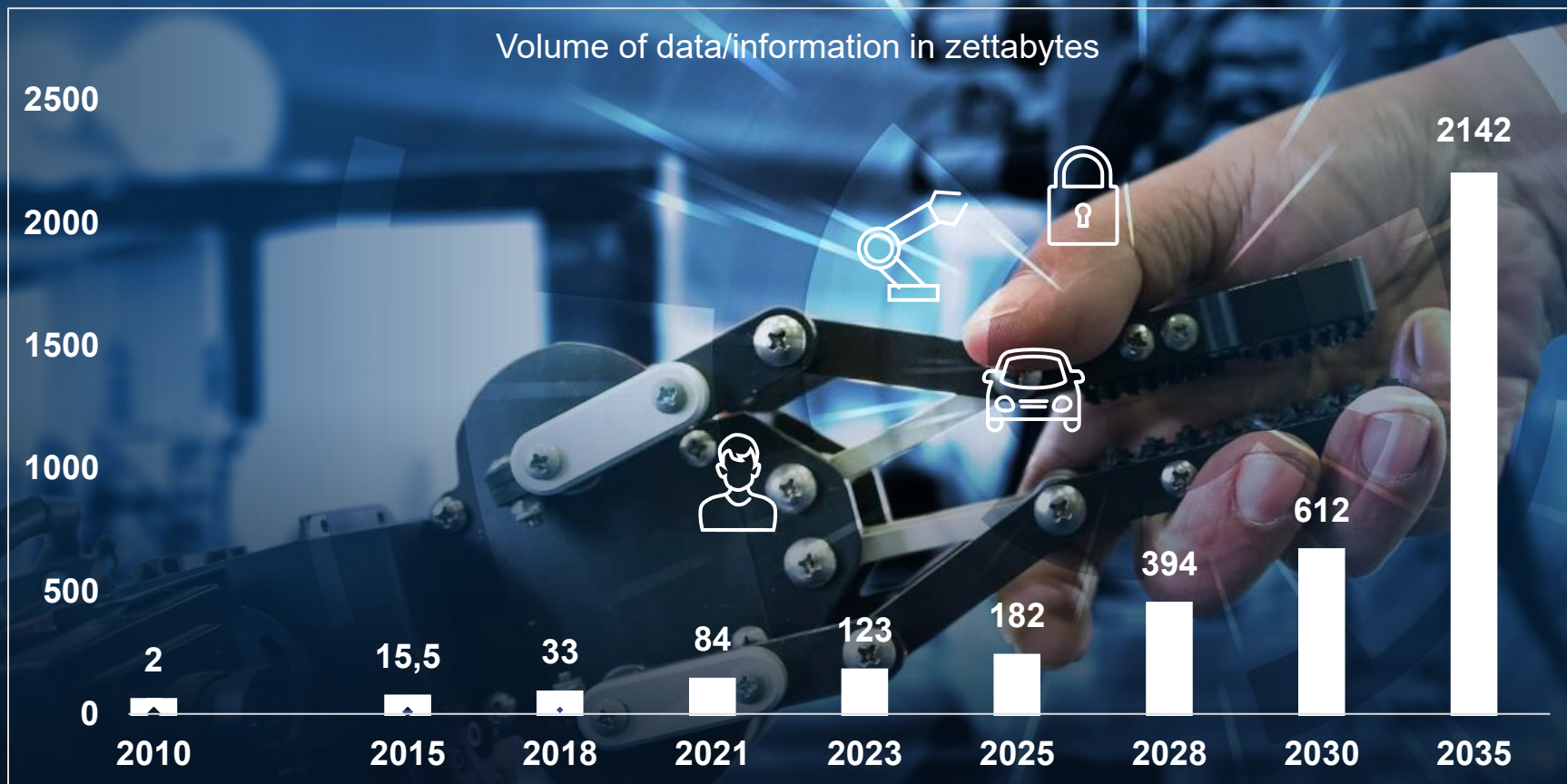
Mobile users
6.4 billion



Internet traffic
33 Exabytes per day

FACING THE DATA DELUGE

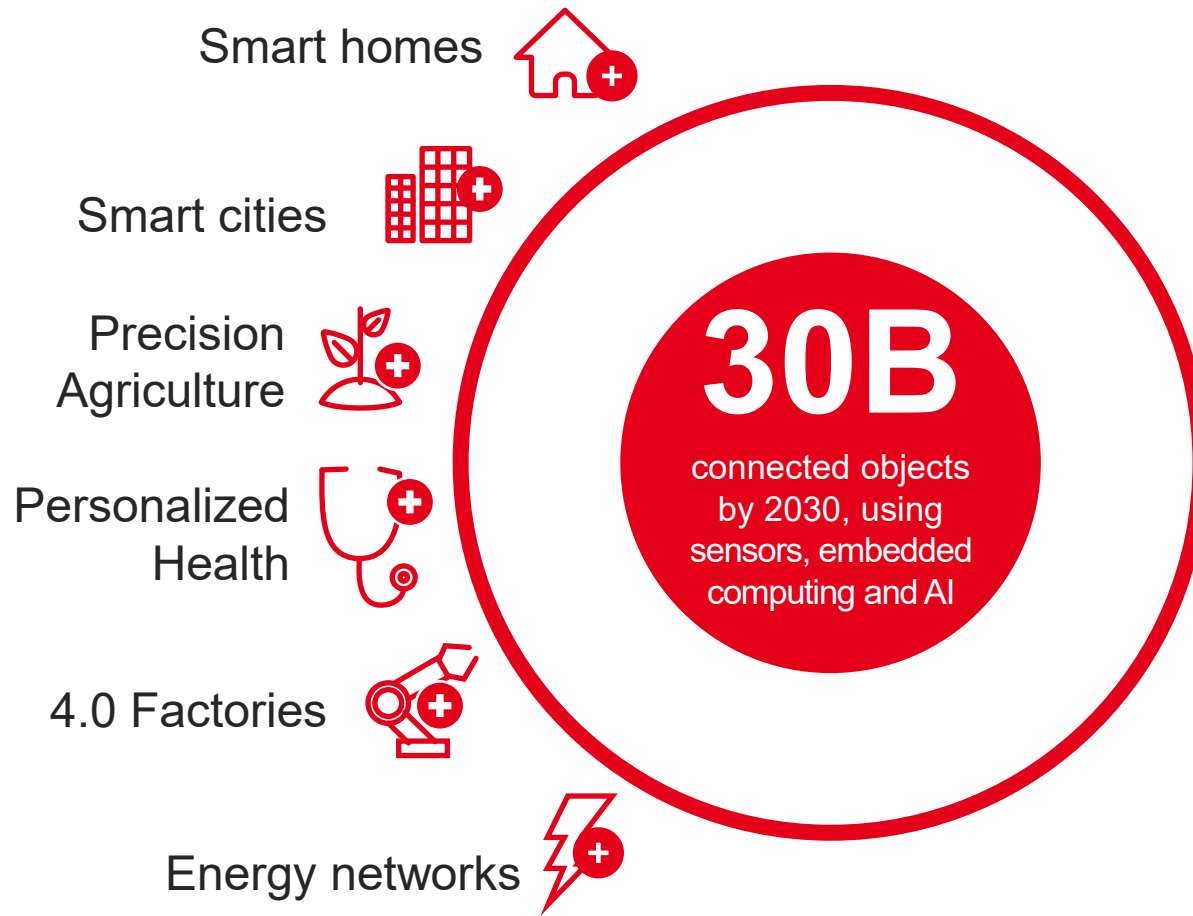
THE YOTTA ERA (10^{24})



90%
of the total data
are generated
by machines in 2025,
vs. only 44% in 2018

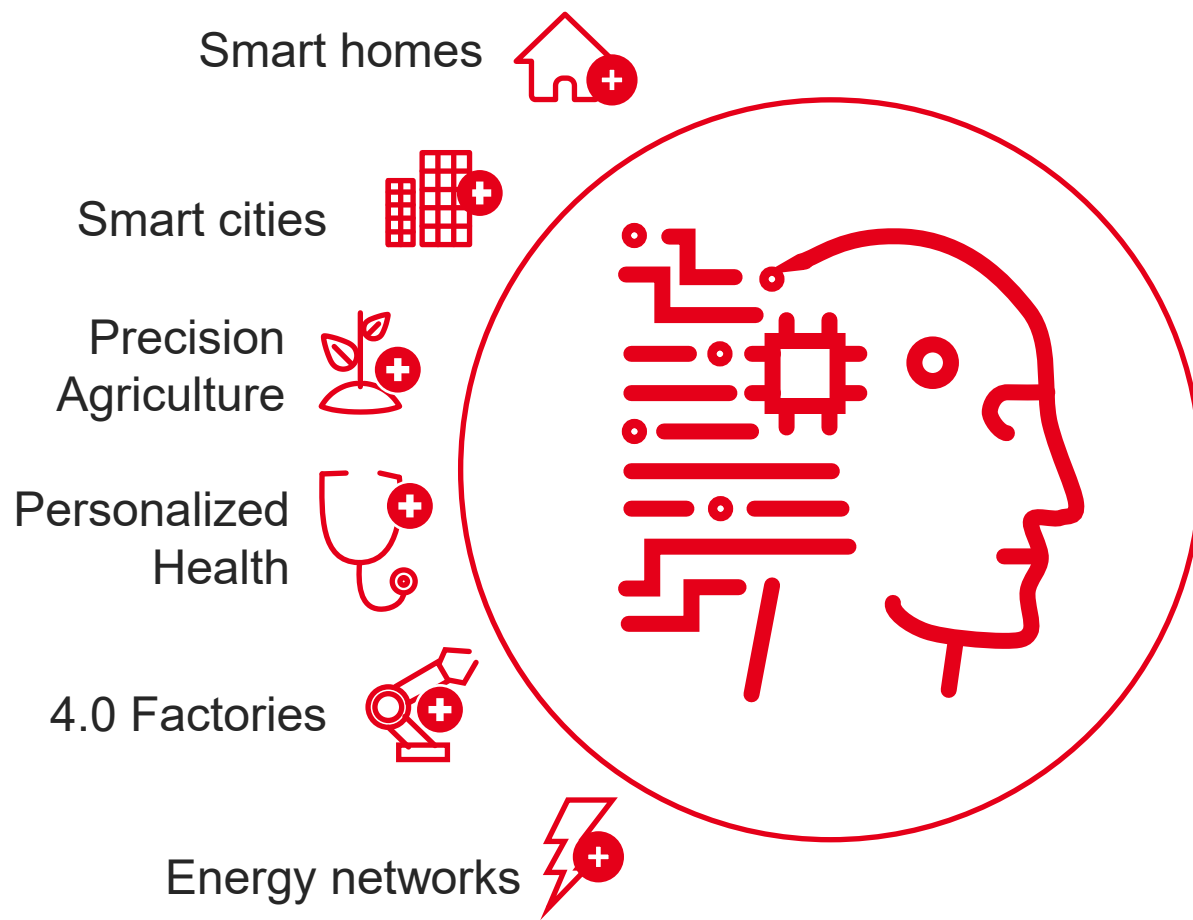
IDC, Statista 2018 and 2025

DIGITALIZING THE ECONOMY TO PROVIDE NEW SERVICES



<https://webdesobjets.fr/etude-gartner-8-milliards-objets-connectes-en-2017/>

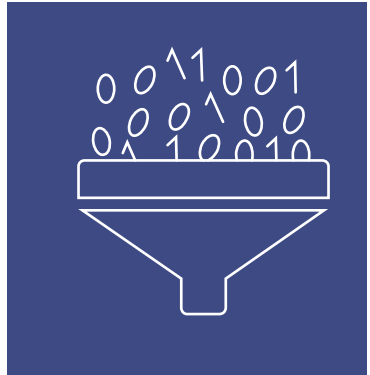
DATA-BASED DIGITALIZATION OF THE ECONOMY



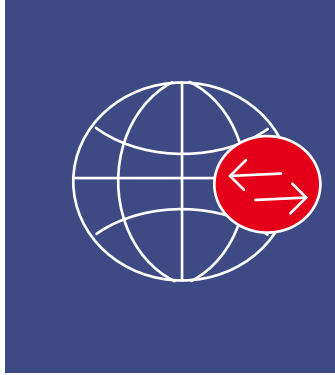
IoT, AI and digital twins will help:

- Run factories and optimize raw materials and energy usage
- Manage decentralized and intermittent energy production
- Design new materials and new medication
- And more

DATA MANAGEMENT AND SERVICES GENERATED



DATA
COLLECTION



DATA
TRANSMISSION



DATA STORAGE
AND ELEMENTARY
PROCESSING



DATA EXPLOITATION

50%

of the data are
real-time by 2025
(dark data)

80%

of data will be
processed locally
or at the edge in
2030

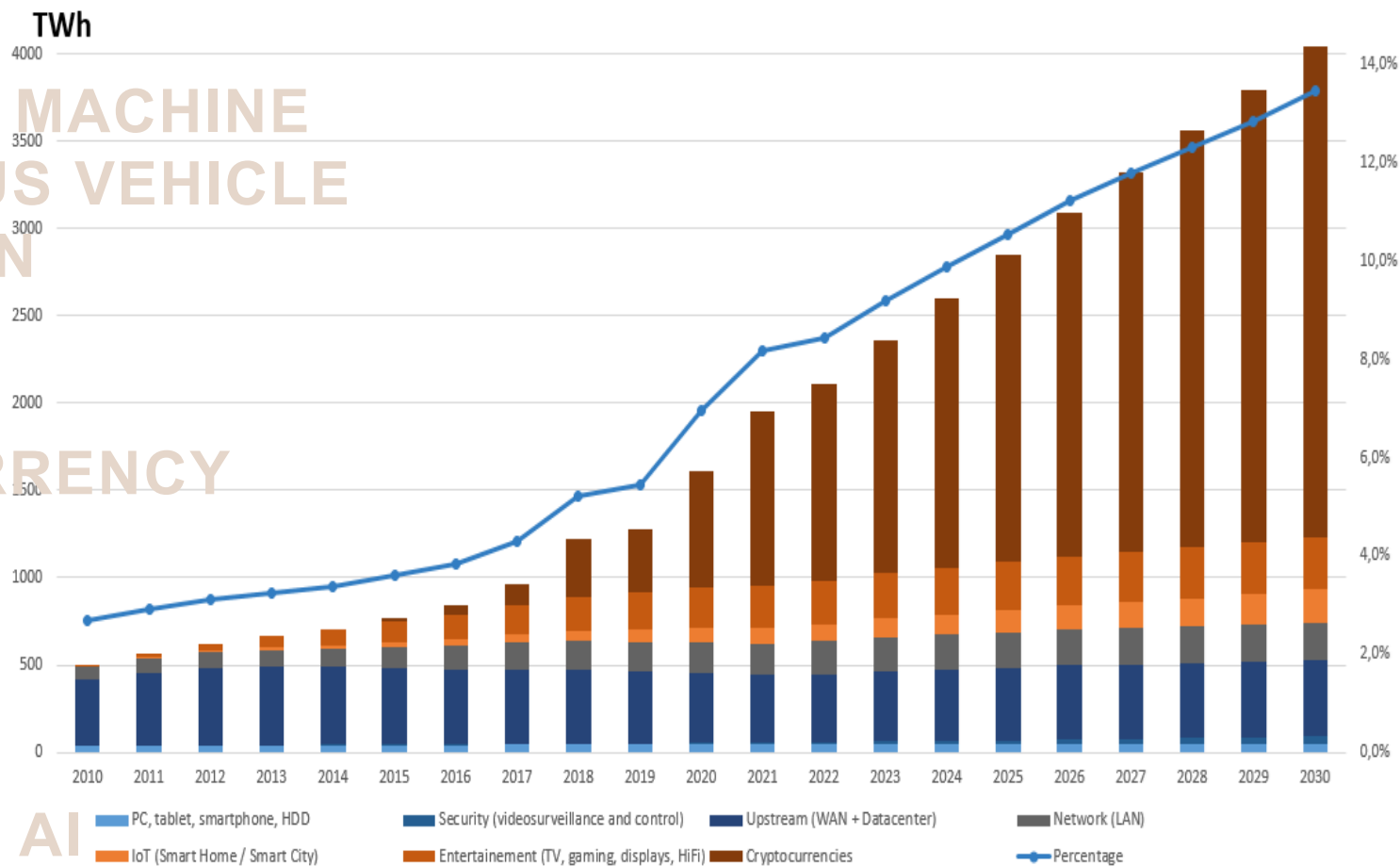
AI will be implemented
in the computing continuum
from edge to cloud:

- Deep edge AI (sensors)
- Edge AI
- AI in the cloud

TOMORROW'S COMPUTING CHALLENGES

A NEW DATA TSUNAMI?

SENSORS
MACHINE TO MACHINE
AUTONOMOUS VEHICLE
BLOCK CHAIN
INDUSTRY
GENOMICS
CRYPTO CURRENCY
HPC
GAMING
NEW SPACE
SMART TV
GENERATIVE AI

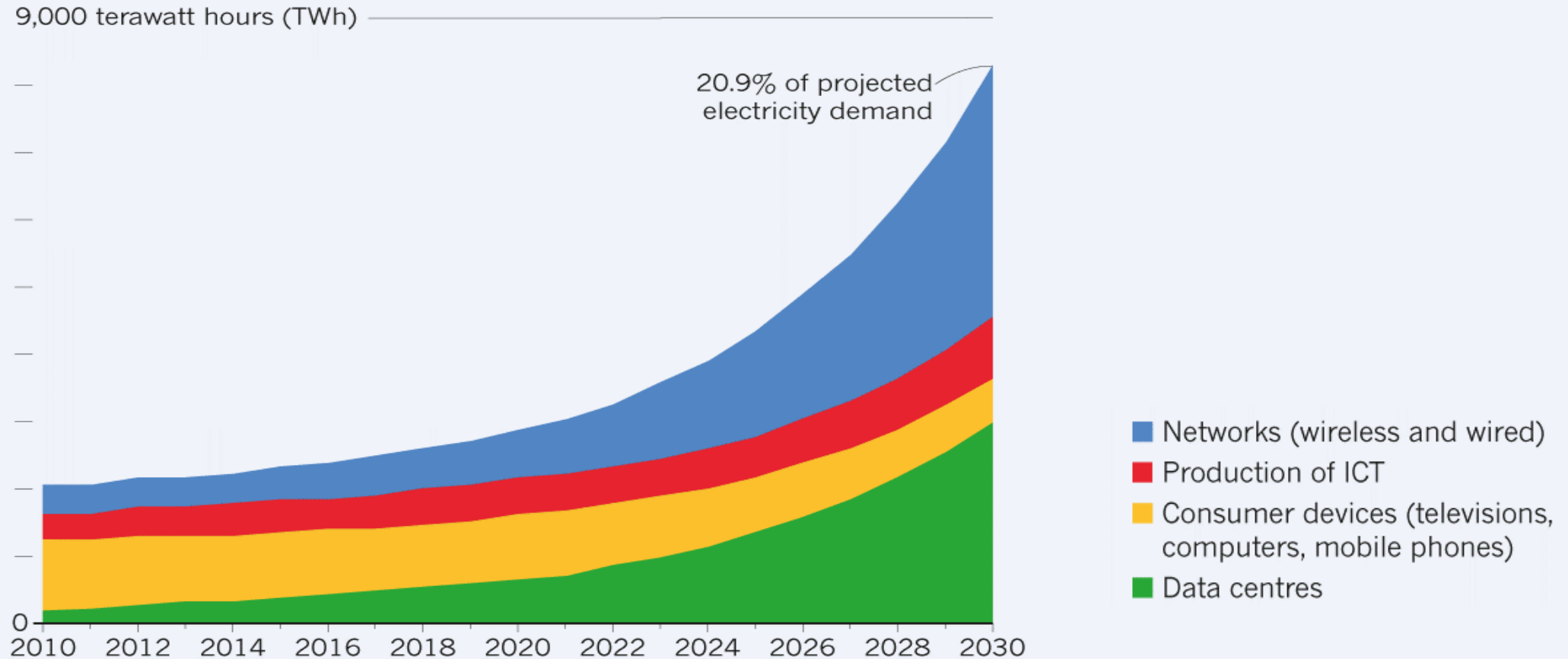


Towards
14%
of the global
electricity demand?

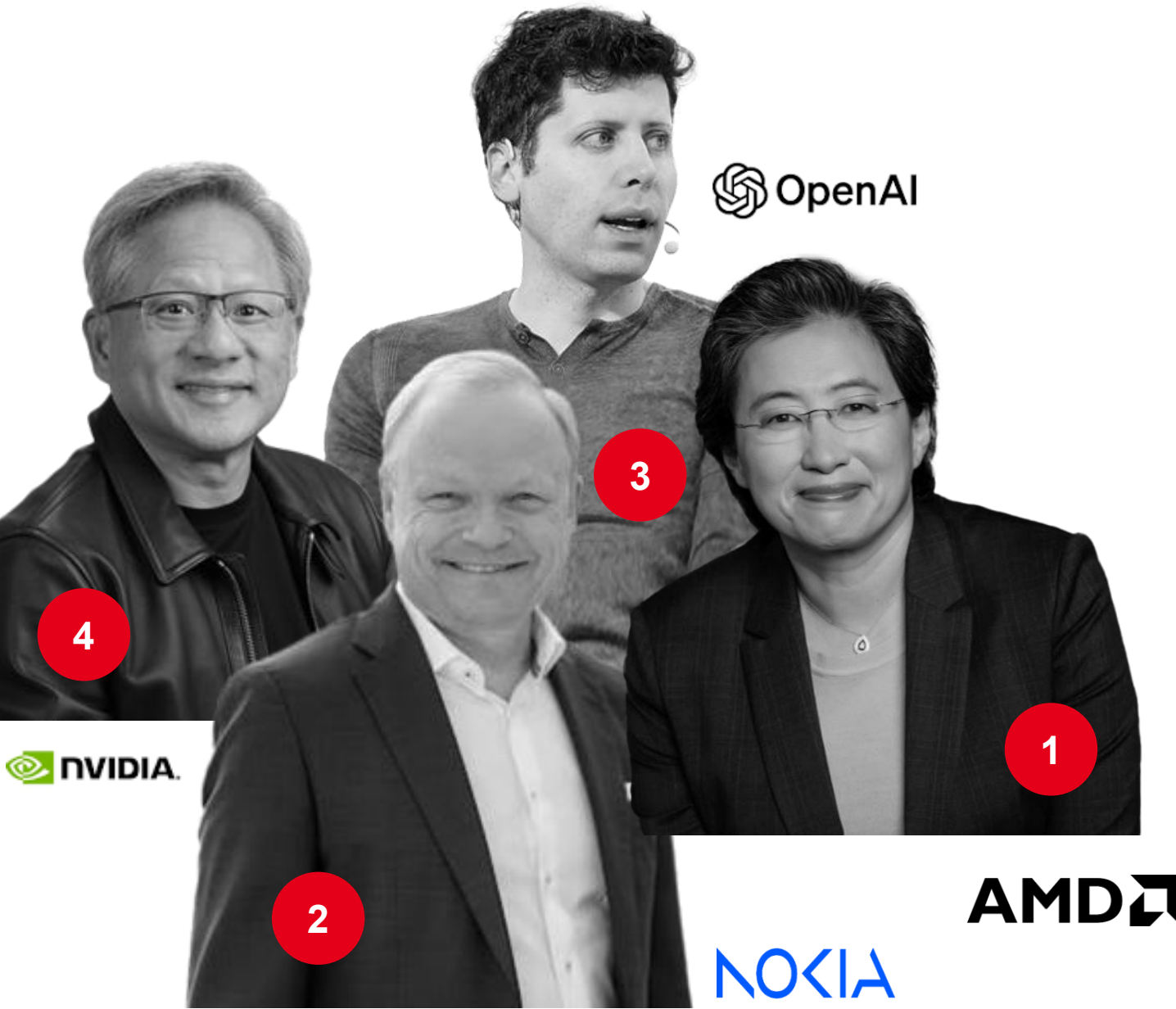
IEA global-electricity-demand-by-scenario-2010-2030, Enerdata, Cambridge Bitcoin Electricity Consumption Index 2021, Total Energy Model V2.0 for Connected Devices EDNA 2021

INFORMATION COMMUNICATION TECHNOLOGIES

ENERGY FORECAST



ENERGY EFFICIENCY IS THE MAIN CHALLENGE



1 **Lisa Su, CEO of AMD** (February 2025)
“Over the next decade, we must think of energy efficiency as the most important challenge”

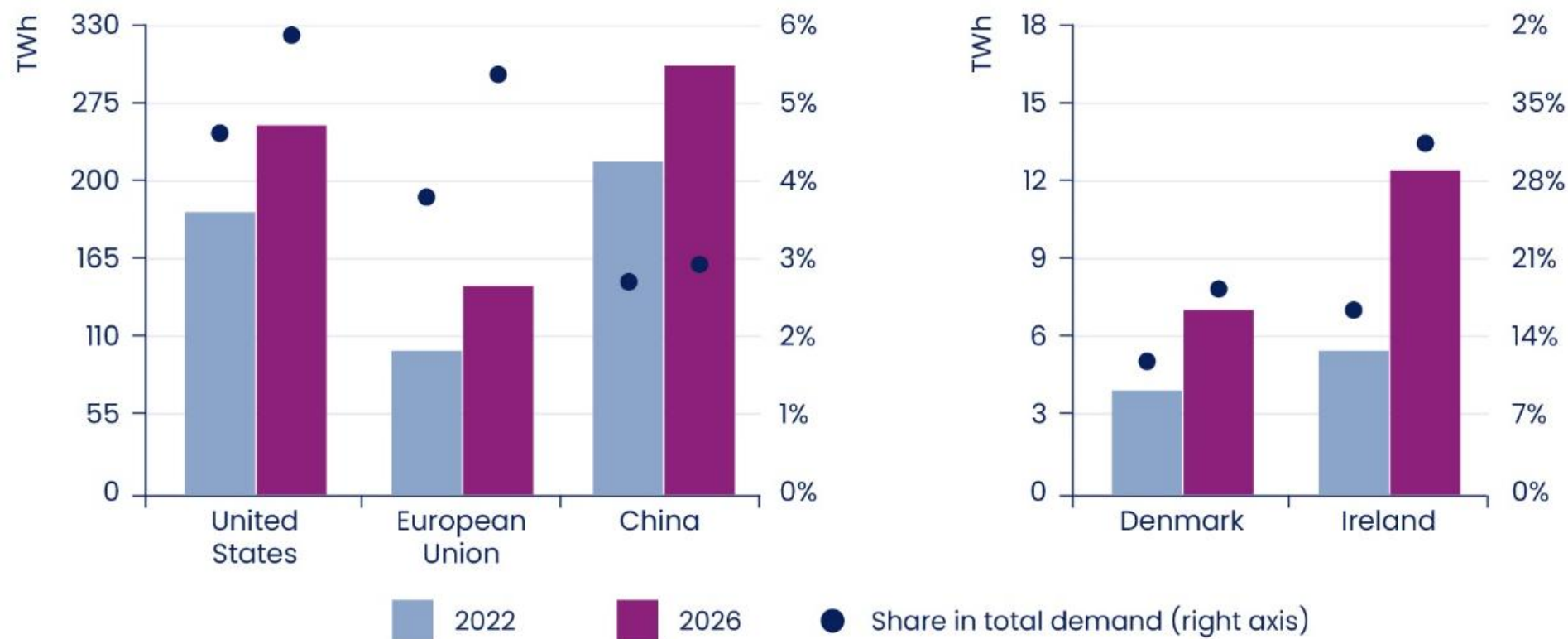
2 **Pekka Lundmark, CEO of Nokia** (January 2025)
“Making AI greener starts with a smarter data center design”

3 **Sam Altman, CEO of OpenAI**
“Future AI depends on energy breakthroughs (Davos, January 2025)”

4 **Jenseng Huang, CEO Nvidia** (September 2024)
“AI will Impact the future of energy”

GLOBAL ELECTRICITY DEMAND GROWTH: THE PART OF DATA CENTERS

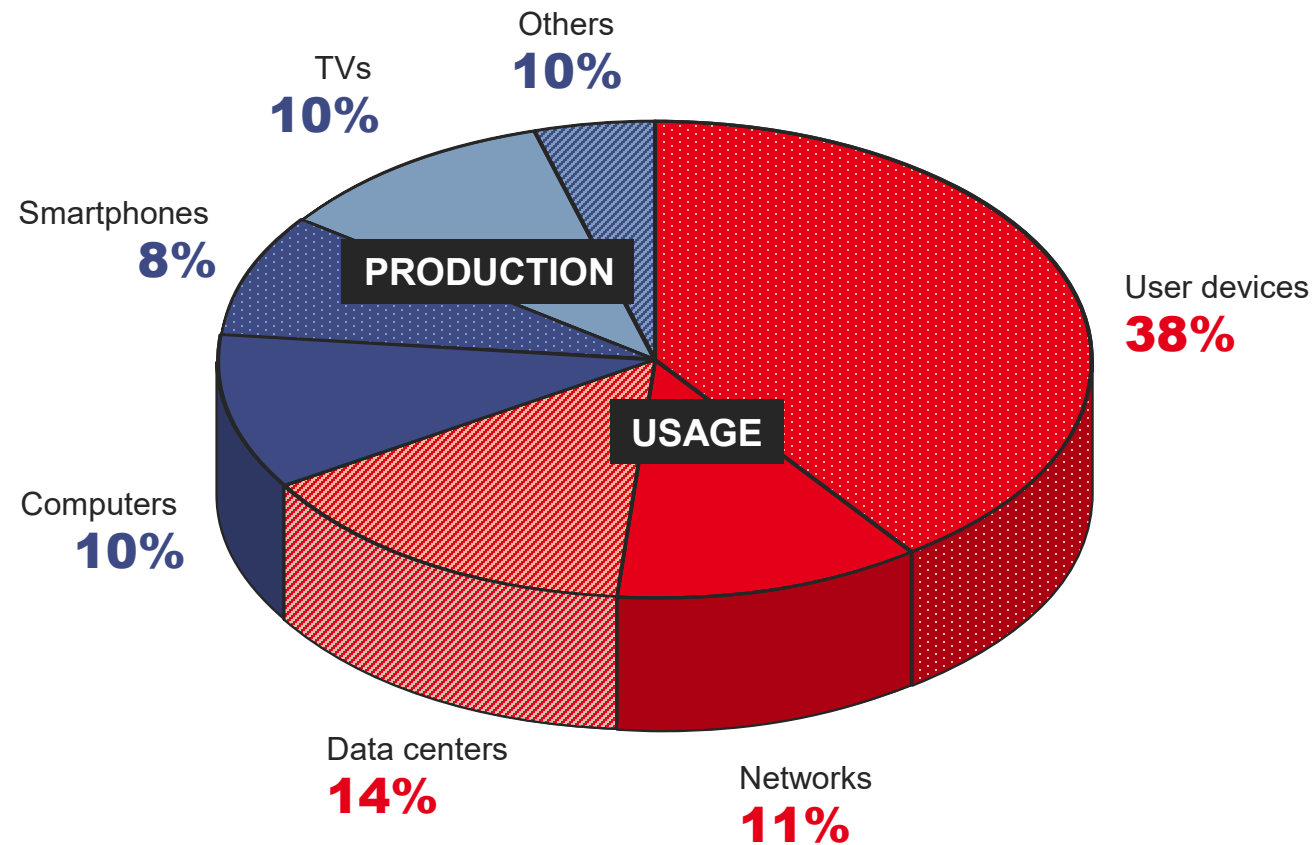
Evolution (2022-2026) and share in total electricity in selected regions



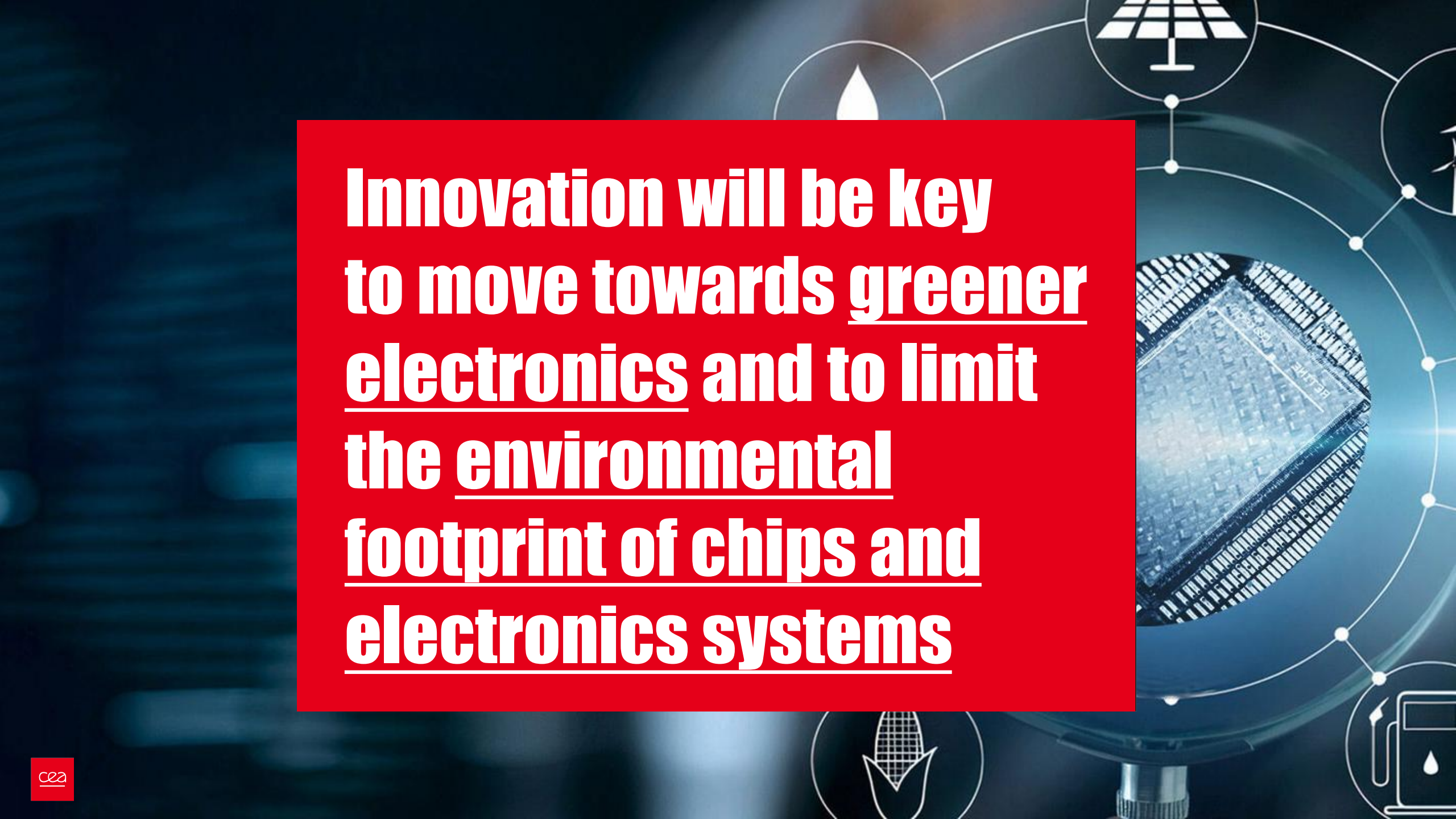
<https://www.iea.org/reports/world-energy-outlook-2024>

REDUCING ENERGY CONSUMPTION IN ELECTRONIC DEVICES: **A TWO-LEVEL APPROACH**

37%
of the energy
is consumed
during **production**



63%
of the energy
is consumed
by using the
devices



**Innovation will be key
to move towards greener
electronics and to limit
the environmental
footprint of chips and
electronics systems**



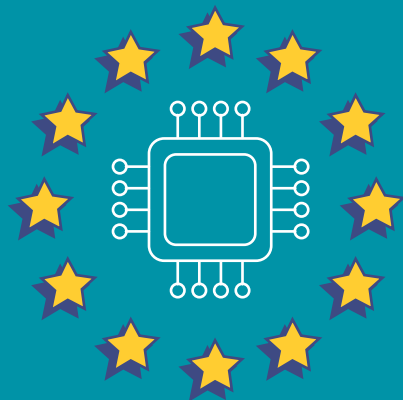
2. ^{Solutions} What can we do?

SOLUTIONS

2

A New Flagship Initiative

Launched by CEA-Leti



R.E.S.O.L.V.E

GREENER CHIPS

ENERGY
EFFICIENCY
GAIN
× 1,000
by 2032

Reducing
Energy consumption for
Sovereignty and
Leadership in
Value-added
Electronics products

15 KEY TECHNOLOGIES TO IMPROVE ENERGY EFFICIENCY

ENERGY
EFFICIENCY
GAIN
× 1,000
by 2032

New
Semiconductors
Technologies

New Memories (embedded, standalone)	3D Heterogeneous Integration & co-Packaged Optics	3D Monolithic, GAA, CFET FD-SOI, 2D Materials	Optical & RF Links (Photonic, GaN LED, mmWave)	Wide Band-gap Power Devices
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Circuits and
Disruptive Chip
Architectures

Energy-efficient HMI (Displays, others)	New Computing Paradigms (Neuromorphic, Analog, Quantum...)	Dedicated Versatile Accelerators	Avoid moving data (Alternative to von Neumann Architectures)	Energy-efficient Power Converters (AC/DC, DC/DC...)
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Systems,
Algorithms,
EDA Tools

Smart Sensors (Deep Edge) Edge AI Computing	New Algorithms (Frugality in Data and Energy)	Sustainable Electronics	AI-based EDA tools STCO⁽¹⁾, ATCO⁽²⁾	Cybersecurity (End-to-End Solutions)
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⁽¹⁾STCO: System Technology Co-Optimization

⁽²⁾ATCO: Application Technology Co-Optimization

ADDRESSING STRATEGIC MARKETS



AUTOMOTIVE



AERONAUTICS



TELECOMS



SMART DATA CENTER



DEFENSE



SPACE



INDUSTRY 4.0



BIOMEDICINE



MEDICAL DEVICES



AGRICULTURE



IoT - SENSORS



DISRUPTIVE HMI

IMPROVING ENERGY EFFICIENCY

15 KEY TECHNOLOGIES

Energy
efficiency
Gain
× 1,000
by 2032

New
Semiconductors
Technologies

New Memories

**3D Heterogeneous
Integration
& co-Packaged
Optics**

**3D Monolithic,
GAA, CFET
FD-SOI,
2D Materials**

Optical & RF Links
(Photonic, GaN LED,
mmWave)

**Wide Band-gap
Power Devices**

Circuits and
Disruptive Chip
Architecture

**Energy-efficient
HMI**
(Displays, others)

**New Computing
Paradigms**
(Neuromorphic,
Analog, Quantum...)

**Dedicated
Versatile
Accelerators**

Avoid moving data
(Alternative to
von Neumann
Architectures)

**Energy-efficient
Power Converters**
(AC/DC, DC/DC...)

Systems,
Algorithms,
EDA Tools

Smart Sensors
(Deep Edge)
Edge AI Computing

New Algorithms
(Frugality in Data
and Energy)

**Sustainable
Electronics**

**AI-based
EDA Tools**

Cybersecurity
(End-to-End Solutions)



R.E.S.O.L.V.E

NEW SEMICONDUCTORS TECHNOLOGIES

A set of new disruptive technologies,
currently under development and ready
to be used by industry

ENERGY
EFFICIENCY
GAIN
× 1,000
by 2032

New Memories

**3D Heterogeneous
Integration
& co-Packaged
Optics**

**3D Monolithic,
GAA, CFET
FD-SOI,
2D Materials**

Optical & RF Links
(Photonic, GaN LED,
mmWave)

**Wide Band-gap
Power Devices**

**Energy-efficient
HMI**
(Displays, others)

**New Computing
Paradigms**
(Neuromorphic,
Analog, Quantum...)

**Dedicated
Versatile
Accelerators**

Avoid moving data
(Alternative to
von Neumann
Architectures)

**Energy-efficient
Power Converters**
(AC/DC, DC/DC...)

Smart Sensors
(Deep Edge)
Edge AI Computing

New Algorithms
(Frugality in Data
and Energy)

**Sustainable
Electronics**

**AI-based
EDA Tools,
STCO, ATCO**

Cybersecurity
(End-to-End Solutions)



leti

Dive into CEA-Leti's world-class semiconductor cleanroom



[Watch the video](#)

09:32



leti



READY-TO-USE FERROELECTRIC MEMORIES

GAIN
@SYSTEM
LEVEL
100

Programming Power
Reduction **×20,000**

FLASH

ReRAM (HfO₂)

FeRAM (HfO₂)

Programming power

~200 pJ/bit

~100 pJ/bit

~10 fJ/bit

Write speed

20 μs

10-100 ns

14 ns @ 2.5 V

Endurance

10⁵ - 10⁶

10⁵ - 10⁶

> 10¹¹

Retention

> 125°C

> 125°C

85°C

Extra masks

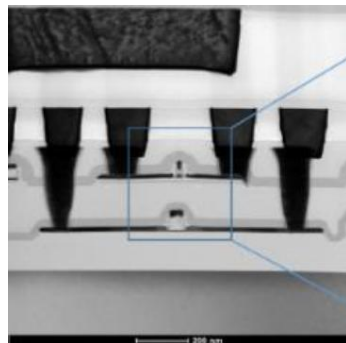
Very high (>10)

Low (2)

Low (2)

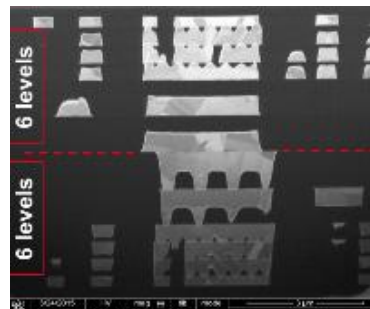
READY-TO-USE 3D-STACKING & PACKAGING

(from device to SIP integration)



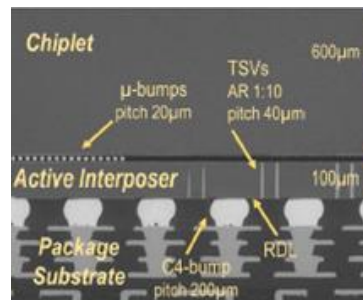
3D sequential Integration

2 tiers including
Photodiodes, LED, high-
and low-temp. transistors



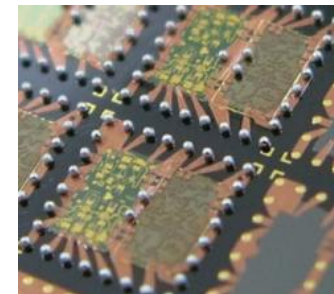
Direct hybrid bonding

Wafer-to-wafer
Min pitch: 1 μm
Die-to-wafer
Min pitch: 4 μm
Self-assembly



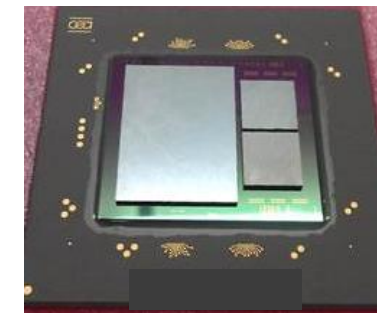
Active interposers

Through-silicon-Vias
TSV 0,3 to 80 mm Φ
RDL 20 μm pitch
Cu pillars 10 mm Φ



Fan-Out-Wafer- Level-Packaging (FOWLP)

Heterogeneous
System-in-Package
Thermal extraction



Die-level packaging

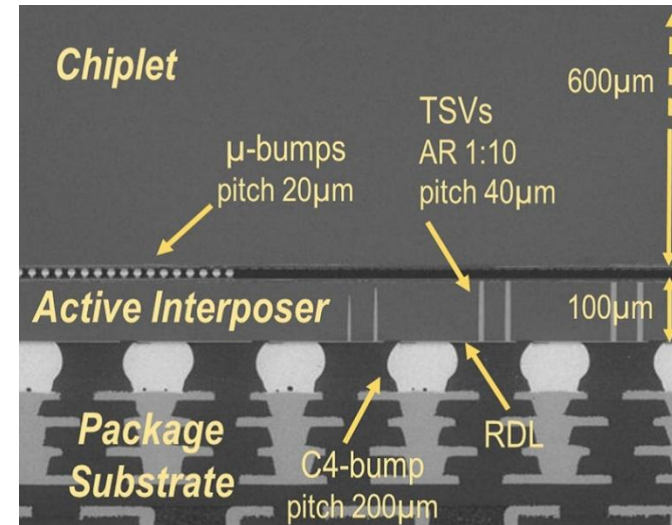
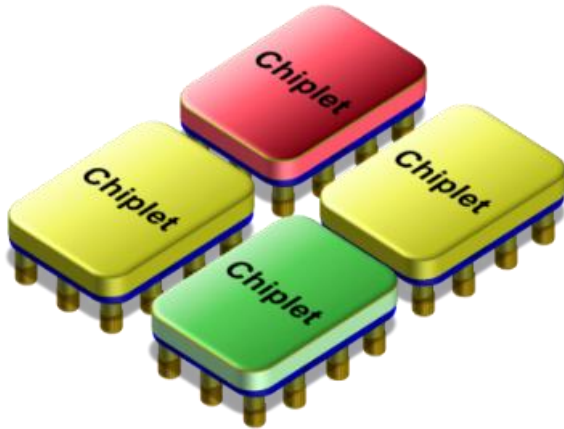
Harsh environments
Power modules
Cryo-packaging for
quantum computing



Large range of interconnect dimensions and materials
from device to system

READY-TO-USE 3D-STACKING TECHNOLOGIES

Chipselets and Active Interposer Integration Demonstrator



Energy
Efficiency
Gain

×10

Concept

- Improve parallelism, reduce power consumption, reduce NRE cost, bring versatility and scalability with a modular architecture based on smaller chips

Achievement

- The power of 10 laptops with a surface of only 200 mm²
- 100 GOPS, 10 GOPS/Watt

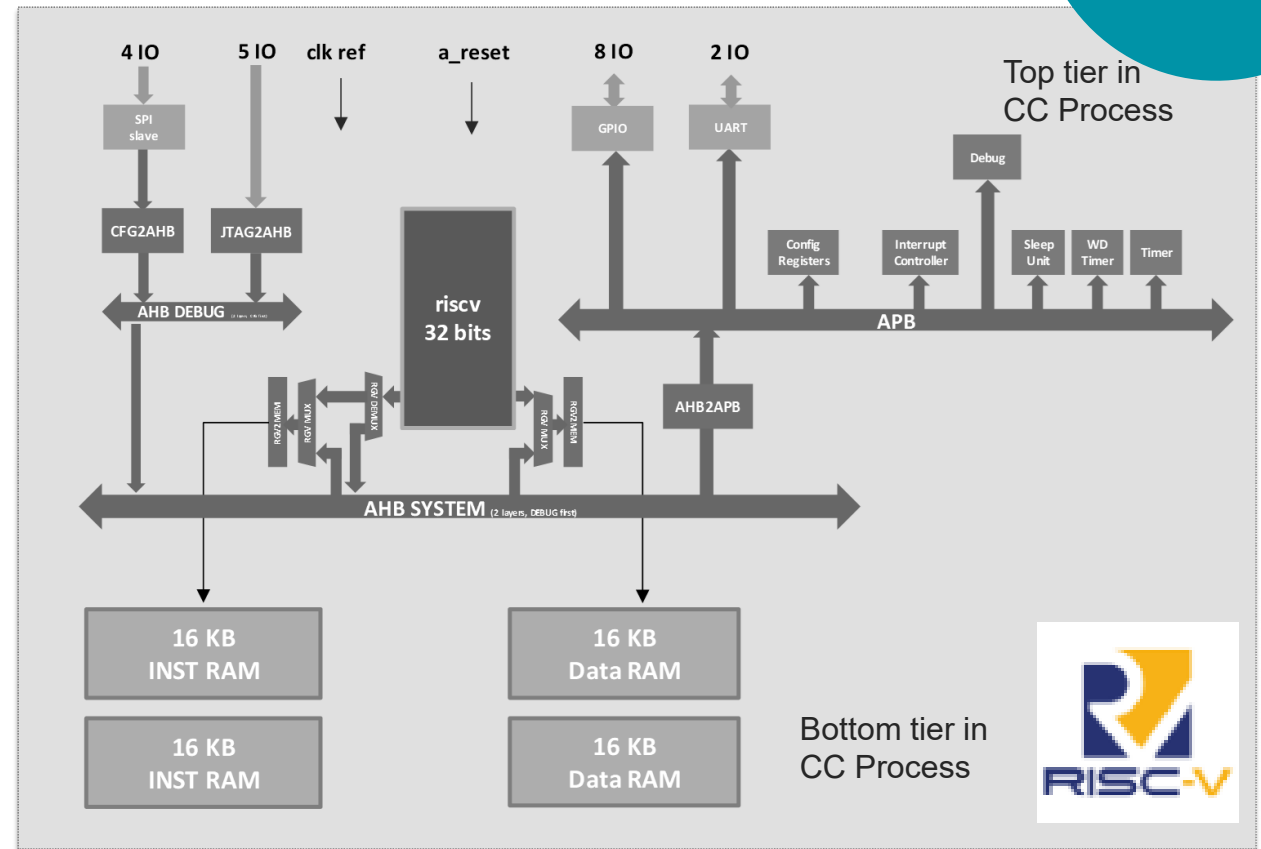
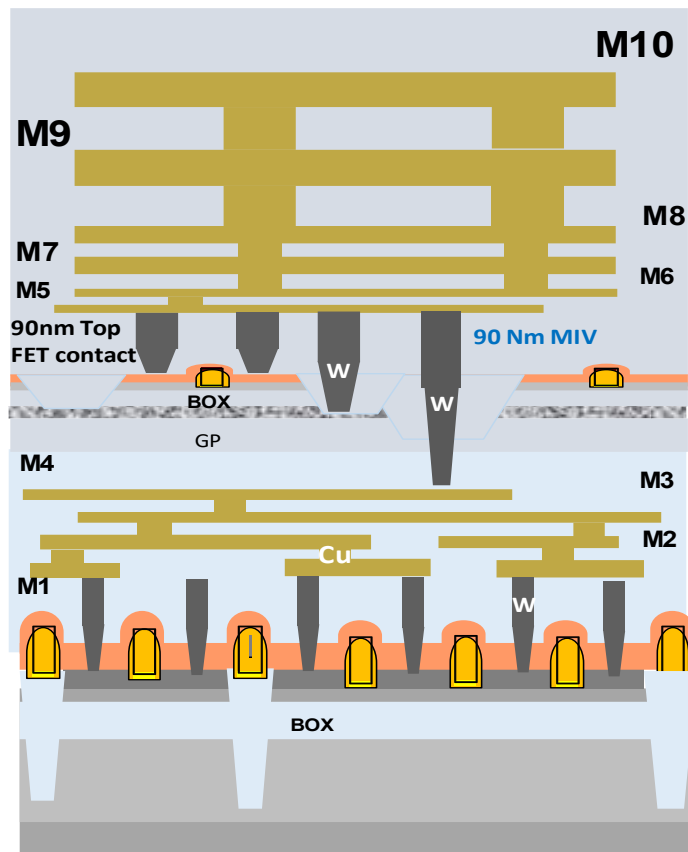
P. Vivet et al., "IntAct: A 96-Core Processor With Six Chiplets 3D-Stacked on an Active Interposer With Distributed Interconnects and Integrated Power Management," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 1, pp. 79-97, Jan. 2021, doi: 10.1109/JSSC.2020.3036341

READY-TO-USE 3D SEQUENTIAL INTEGRATION

CoolCube 3D Sequential Integration Technology

Energy
Efficiency
Gain

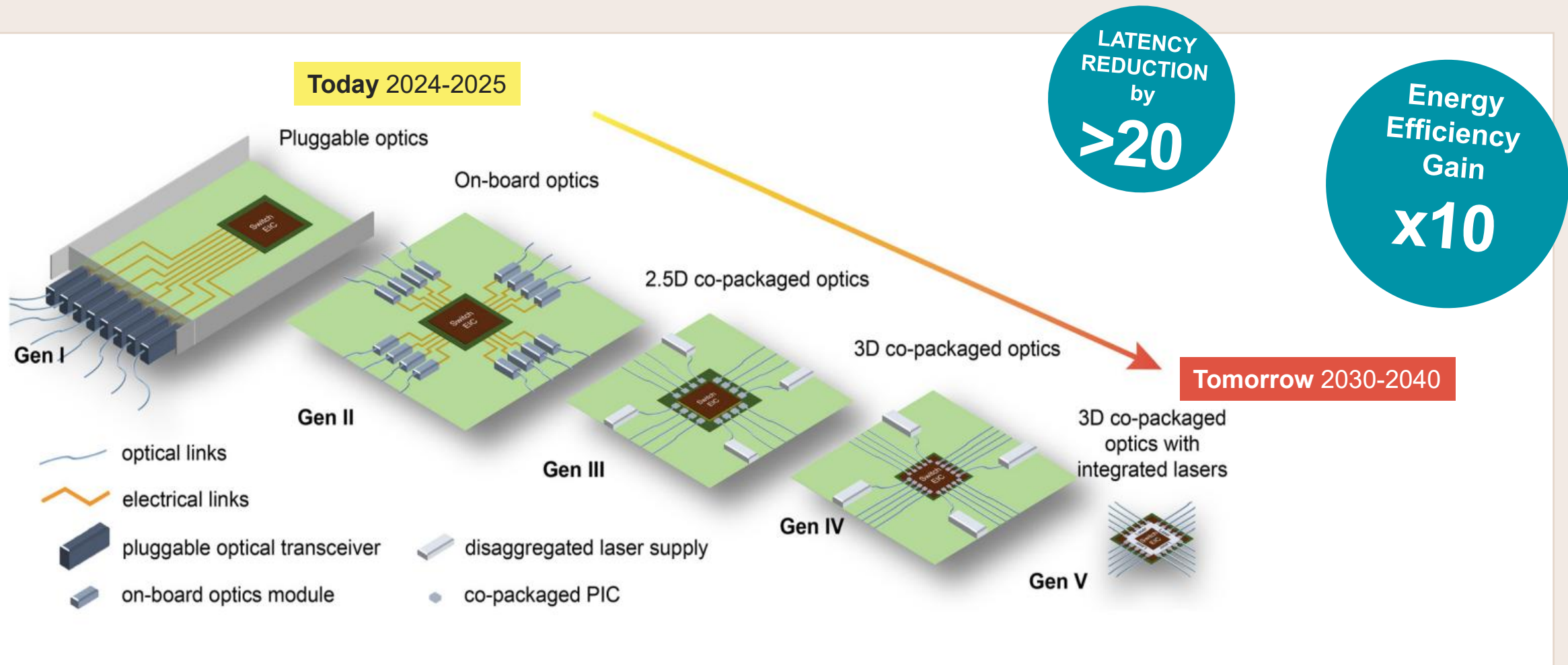
×2-10



O. Billoint, K. Azizi-Mourier, G. Cibrario, D. Lattard, M. Mouhdach, S. Thuries, P. Vivet, "Merging PDKs to Build a Design Environment for 3D Circuits: Methodology, Challenges and Limitations, IEEE International 3D Systems Integration Conference (3DIC), Sendai, Japan, October 2019

ADDRESSING HPC & AI CHALLENGES (EIC, PIC)

A MOVE TO CO-PACKAGED OPTICS (CPO)



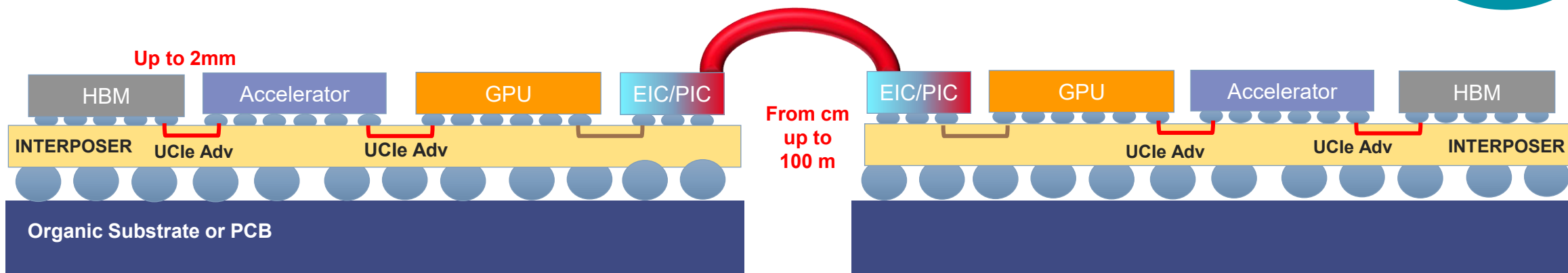
Appl. Phys. Lett. 2021 (Broadcom, UCSB, Intel)

ADDRESSING HPC & AI CHALLENGES WITH OPTICAL INTERCONNECTS

Energy
Efficiency
Gain using
LED

~10

Electro-optical Communication Between Chiplet-based Circuits



Silicon Photonics Serial Link

Mature technology

- ▶ **Very-high Data Rate (DR)** per Optical Fiber
- ▶ DR/Fiber: 400/800/1600 Gbps for 8 wavelength
- ▶ High-complexity transceiver (linear)
- ▶ Medium latency
- ▶ Energy efficiency: 3 to 5 pJ/bit



μLED/μPD Array Highly Parallel Link

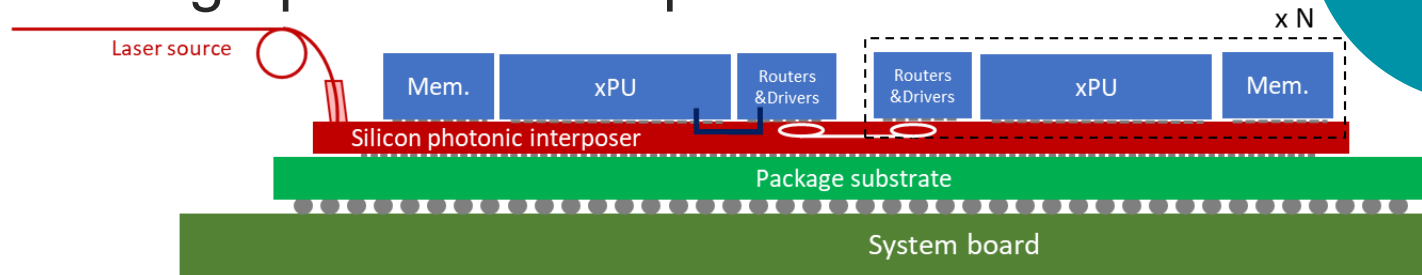
Disruptive technology

- ▶ **1 to 4 Gb/s per MicroLED**
- ▶ **Combined with parallelization: >10 Tb/s/mm²**
- ▶ **Very-low latency**
- ▶ **Energy efficiency: 0.5 pJ/bit**

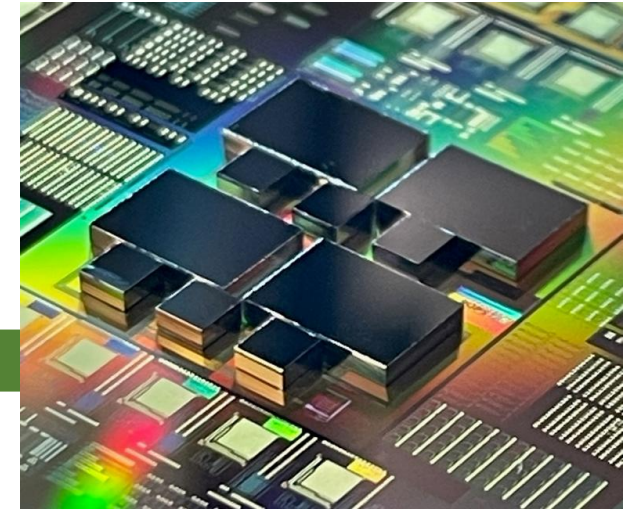
A WORLD FIRST : A PHOTONIC INTERPOSER WITH AN OPTICAL NETWORK-ON-CHIP (O-NOC)

STARAC DEMONSTRATOR

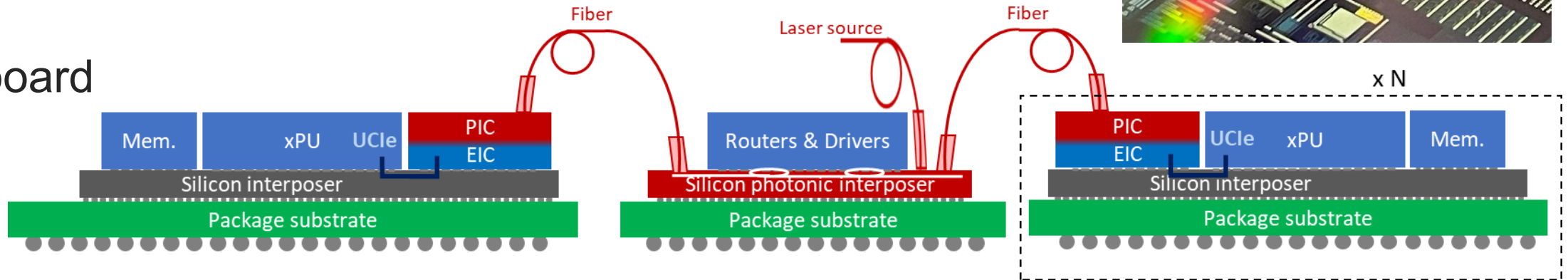
On large photonic interposer



Energy
Efficiency
Gain
×3.5



On board



CIRCUITS AND DISRUPTIVE CHIP ARCHITECTURES

New computing and partitioning paradigms
under development and ready to be used by industry

ENERGY
EFFICIENCY
GAIN
× 1,000
by 2032

New Memories

3D Heterogeneous
Integration
& co-Packaged
Optics

3D Monolithic,
GAA, CFET
FD-SOI,
2D Materials

Optical & RF Links
(Photonic, GaN LED,
mmWave)

Wide Band-gap
Power Devices

Energy-efficient
HMI
(Displays, others)

**New Computing
Paradigms**
(Neuromorphic,
Analog, Quantum...)

**Dedicated
Versatile
Accelerators**

Avoid moving data
(Alternative to
von Neumann
Architectures)

Energy-efficient
Power Converters
(AC/DC, DC/DC...)

SPECIALIZED ARCHITECTURES LEAD TO MORE EFFICIENCY

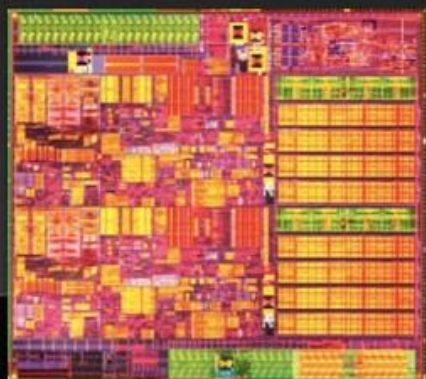
Energy
Efficiency
Gain

×150

CPU

1690 pJ/flop

Optimized for Latency
Caches

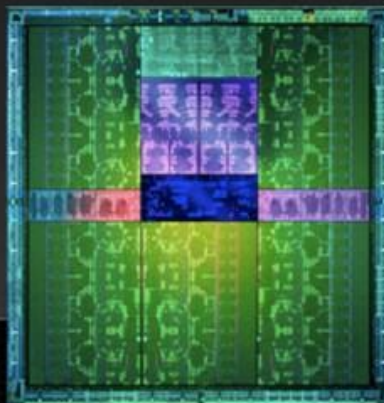


Westmere
32 nm

GPU

140 pJ/flop

Optimized for Throughput
Explicit Management
of On-chip Memory



Kepler
28 nm

Type of device	Energy / Operation
CPU	1690 pJ
GPU	140 pJ
Fixed function	10 pJ

The more you specialize,
the more you gain in energy
efficiency

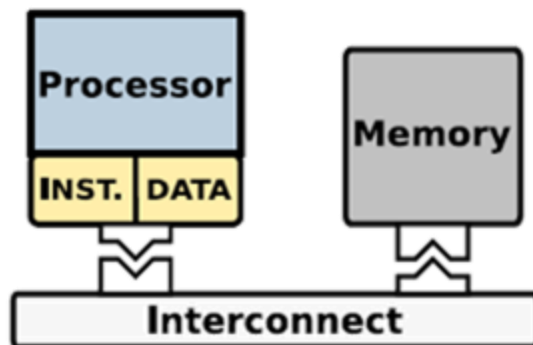
From Bill Dally (nVidia) "Challenges for Future Computing Systems", HiPEAC conference 2015

ADDRESSING THE ENERGY CHALLENGE WITH NEW NON-VOLATILE MEMORIES

Energy
Efficiency
Gain

×10

Von Neumann

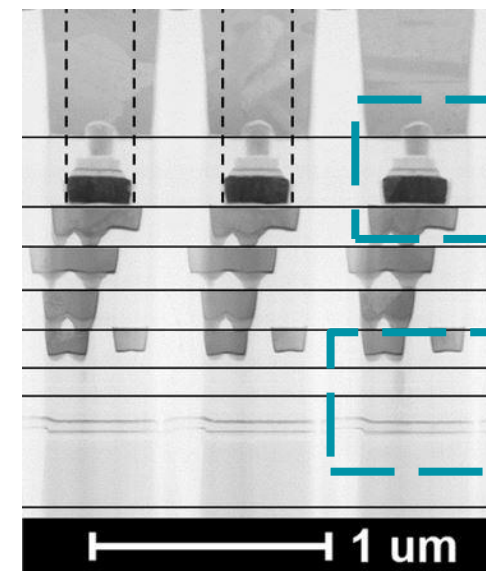


How data consumes energy

Operation	Energy
Addition of data (fixed point)	1×
Accessing data (onchip cache)	60×
Accessing data (offchip RAM)	3500×

Data movement
between storage
and processing
units consumes

90%
of the energy



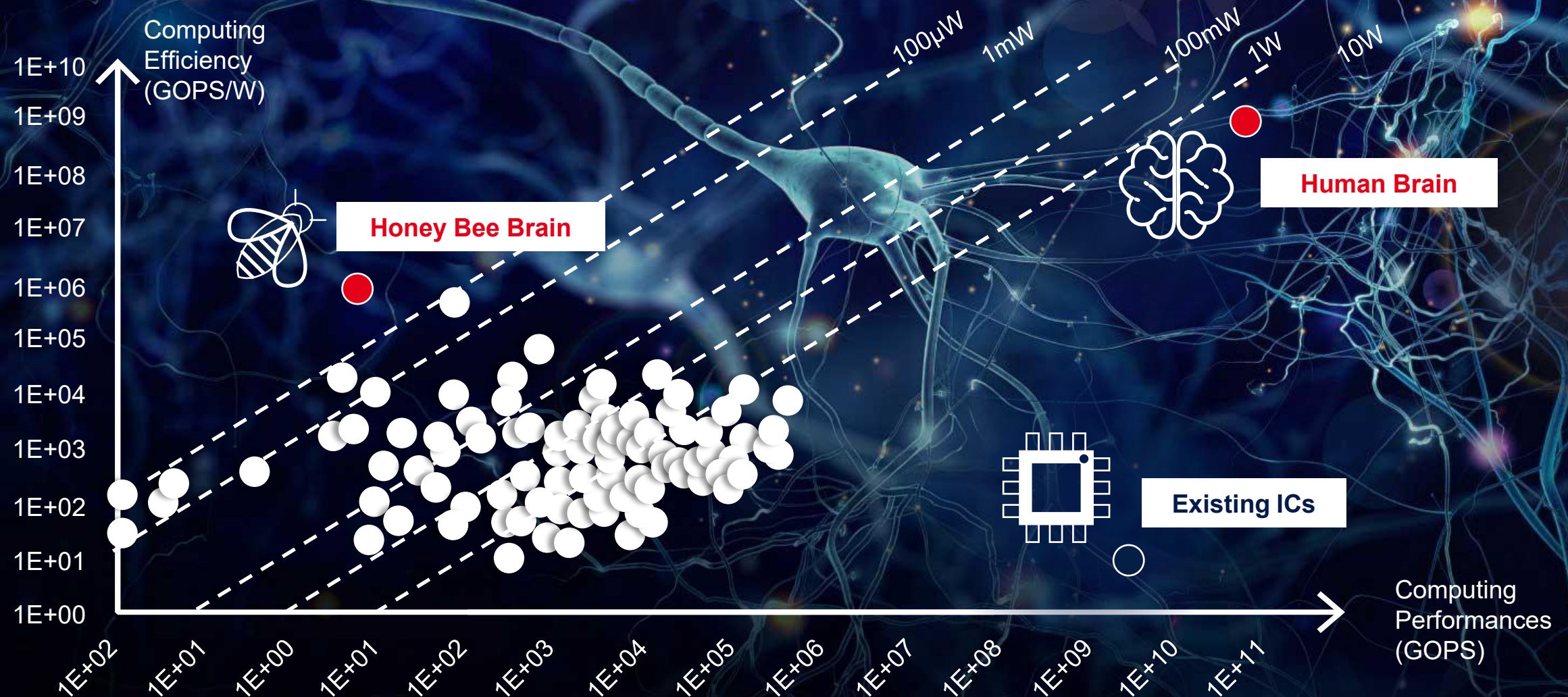
Resistive
memory

FD-SOI

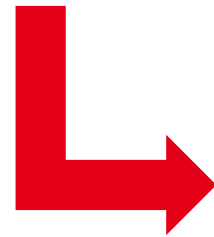
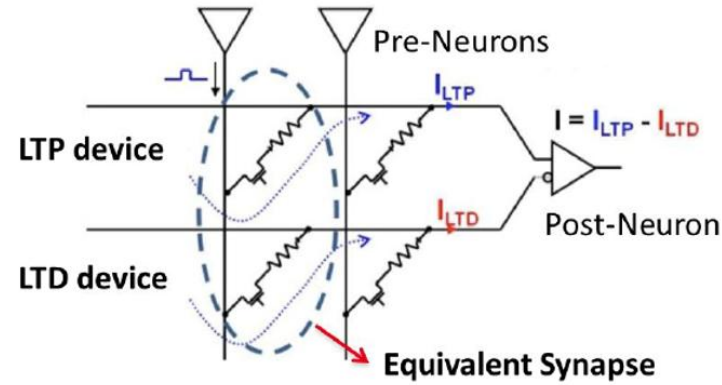
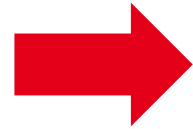
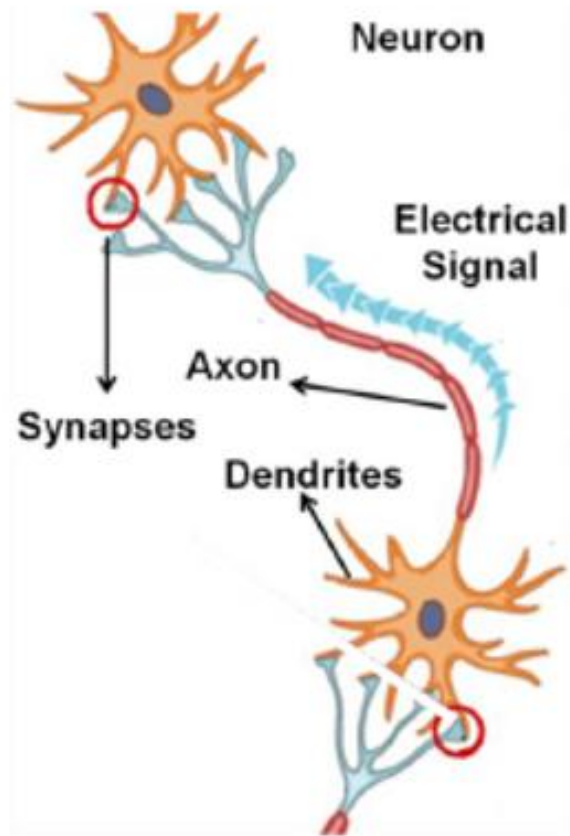
**High-density on-chip non-volatile
memories are needed**

ENERGY EFFICIENCY: FAR BEHIND BIOLOGICAL SYSTEMS

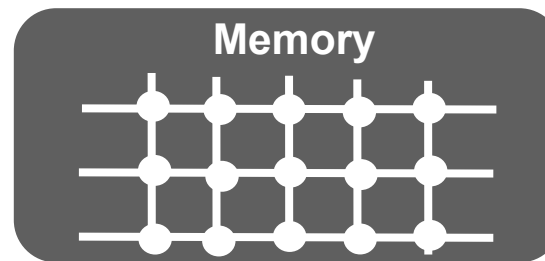
NATURE IS A SOURCE OF INSPIRATION



MIMICKING THE BRAIN'S BEHAVIOR WITH NEUROMORPHIC-BASED RRAM CIRCUITS



Von Neumann Computing

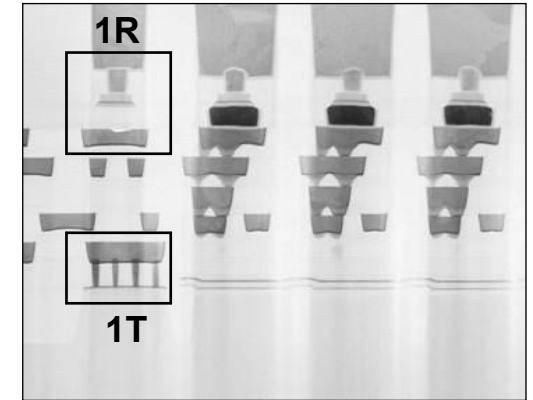
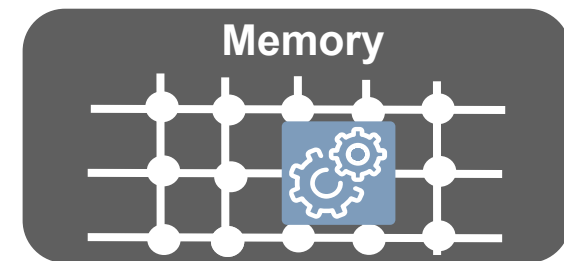


input-data D

results $f(D)$

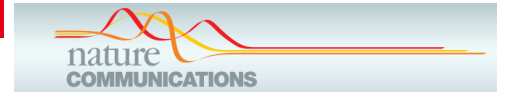


In-Memory Computing

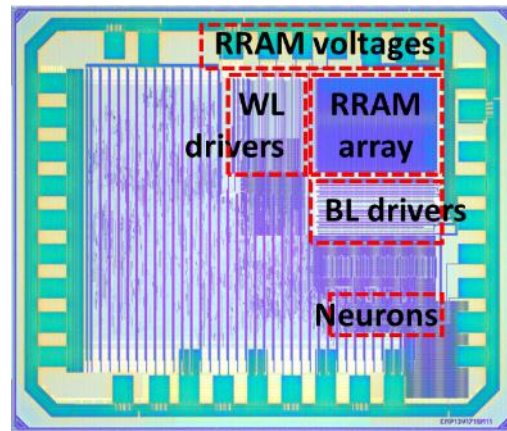


BRAIN-INSPIRED SPIKING NEURAL NETWORK TO REDUCE ENERGY CONSUMPTION

From SPIRIT to LARGO Analog Asynchronous Spiking Neural Networks



SPIRIT



130 nm

CMOS node

10

Nb of Neurons

144

Nb of Synapses

3,6 pJ

Energy / spike

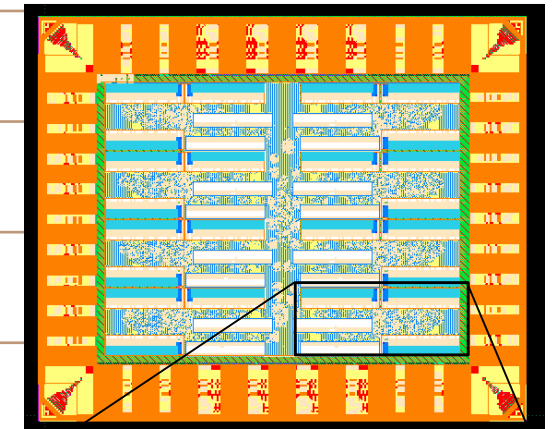
1

Nb of cores

5 mm²

Die size

LARGO



28 nm

131 k

75 M

0,5 pJ

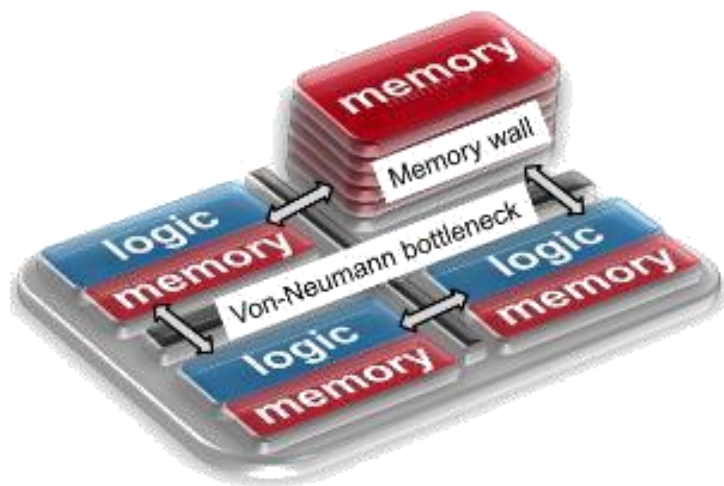
8

3 mm²

SPIRIT: A. Valentian, F. Rummens, E. Vianello, T. Mesquida, C. Lecat-Mathieu de Boissac, O. Bichler, C. Reita, "Fully Integrated Spiking Neural Network with Analog Neurons and RRAM Synapses," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, December 2019

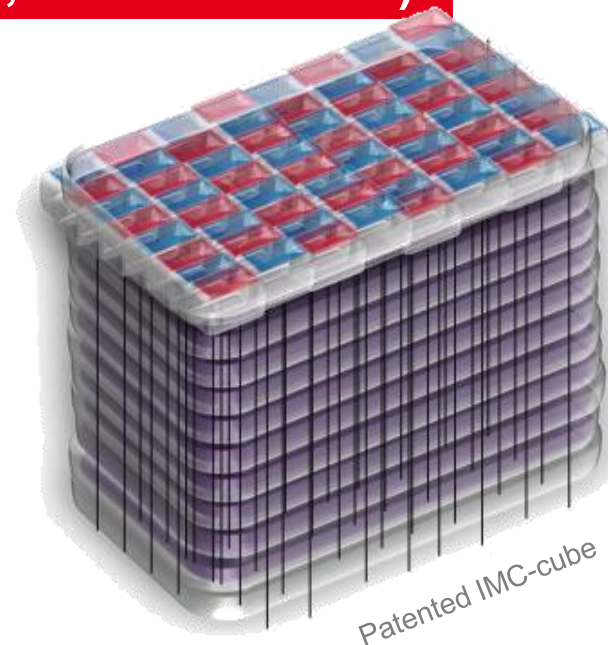
TOWARDS THE ULTIMATE IN-MEMORY COMPUTING

ERC MYCUBE (12 patents, 16 publications, 2 Best Awards)



The problem today

- ▶ Energy efficiency in data-abundant integrated circuits



A solution for tomorrow

- ▶ Highly parallel in-memory computing

Energy
Efficiency
Gain

×100

- Vertical memories
- 3D stacks
- Vertically stacked nanowires
- Circuit demonstrators
- Software tools



SYSTEMS, ALGORITHMS AND EDA TOOLS

Cost-effective solutions
for significant energy savings

ENERGY
EFFICIENCY
GAIN
× 1,000
by 2032

New Memories

3D Heterogeneous
Integration
& co-Packaged
Optics

3D Monolithic,
GAA, CFET
FD-SOI,
2D Materials

Optical & RF Links
(Photonic, GaN LED,
mmWave)

Wide Band-gap
Power Devices

Energy-efficient
HMI
(Displays, others)

New Computing
Paradigms
(Neuromorphic,
Analog, Quantum...)

Dedicated
Versatile
Accelerators

Avoid moving data
(Alternative to
von Neumann
Architectures)

Energy-efficient
Power Converters
(AC/DC, DC/DC...)

Smart Sensors
(Deep Edge)
Edge AI Computing

New Algorithms
(Frugality in Data
and Energy)

Sustainable
Electronics

AI-based
EDA Tools,
STCO, ATCO

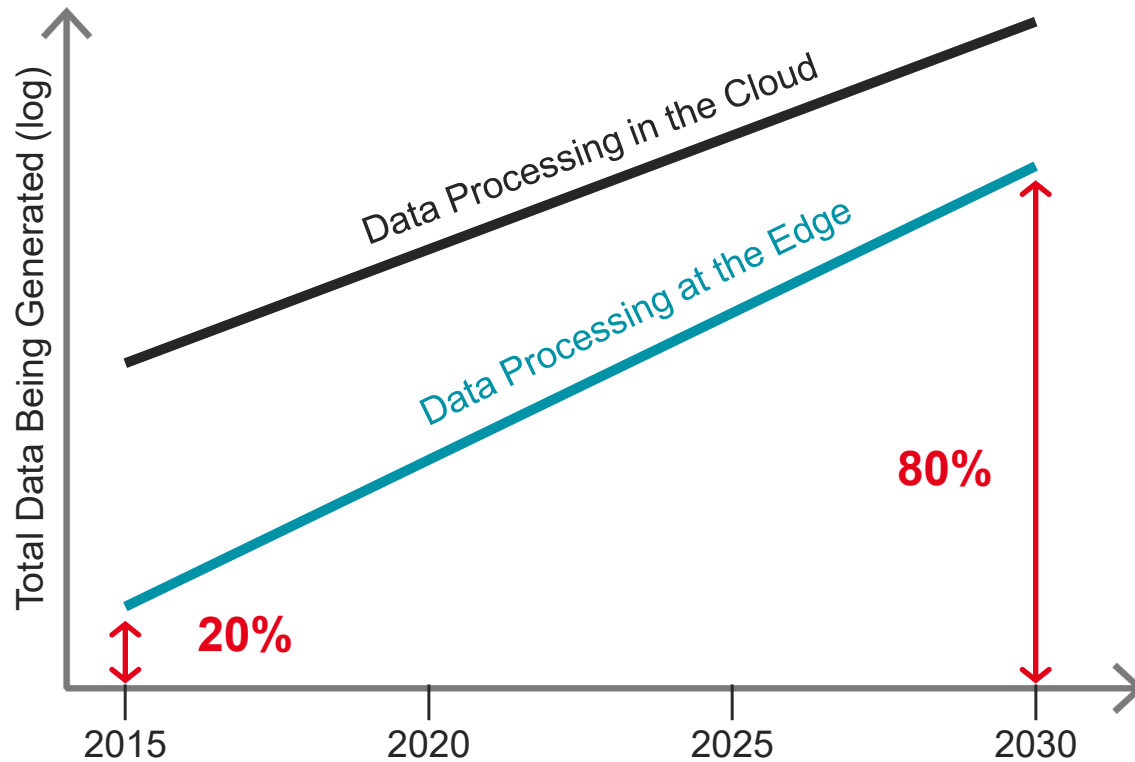
Cybersecurity
(End-to-End Solutions)

TOWARDS ENERGY-EFFICIENT SOLUTIONS

EDGE-AI SOLUTIONS

Energy
Efficiency
Gain

10^6



International Business Strategies, Inc. (IBS) – sept 2020

Transferring or storing 1 GB of data through the Internet uses ~5 kWh,
instead of 5×10^{-6} kWh if done locally

Benefits of Local Processing:

- ▶ Reduce network bandwidth
- ▶ Lower latency
- ▶ Reduce overall energy consumption
- ▶ No need for cloud connection
- ▶ Ensure data protection

TOWARDS EFFICIENT EDGE-COMPUTING SOLUTIONS

The N2D2 Deep Learning Platform

Energy
Efficiency
Gain

~10



**A software tool to explore DNN
with hardware constraints :**

- ▶ Computing power
- ▶ Memory
- ▶ Data accuracy
- ▶ Power consumption

...and develop energy-optimized
perception algorithms for ADAS

list.cea.fr/en/page/n2d2-design-and-implementation-of-neural-networks-optimized-for-embedded-systems/



CHALLENGE

2

Sustainability & Sovereignty

Toward resilient chip manufacturing

THE SEMICONDUCTOR INDUSTRY'S GROWING NEED FOR ELEMENTS

1 H																	2 He				
3 Li	4 Be													5 B	6 C	7 N	8 O	9 F	10 Ne		
11 Na	12 Mg													13 Al	14 Si	15 P	16 S	17 Cl	18 Ar		
19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr				
37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe				
55 Cs	56 Ba	57 La	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn				
87 Fr	88 Ra																				
		58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu						
		90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr						

1980s 1990s 2000s

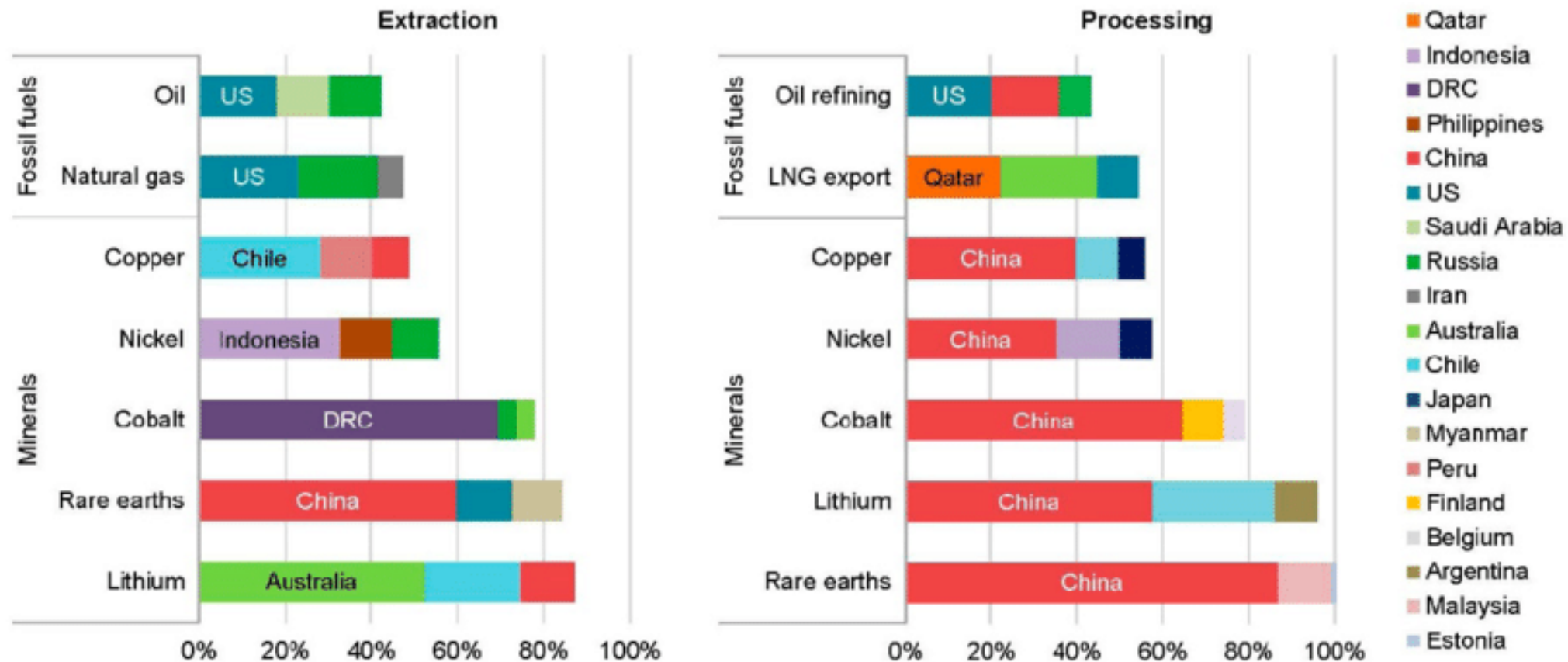
15%

of the elements
used by the semi-
conductor industry

15%
of the elements
used by the semi-
conductor industry
is recycled

MINERAL SOURCING

CHINA'S DOMINANT PROCESSING POSITION



Share of top three producing countries in production of selected minerals and fossil fuels, 2019

LNG = Liquefied natural gas; The values for copper processing are for refining operations

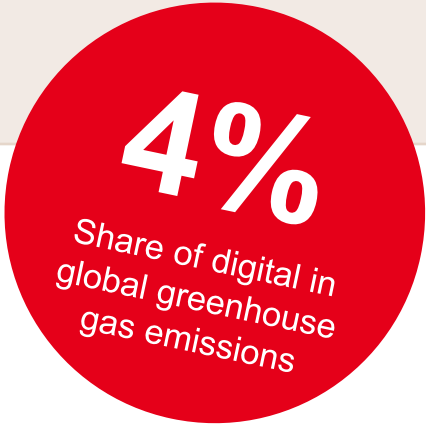
Sources: IEA (2020); USGS (2021), World Bureau of Metal Statistics (2020); Adamas Intelligence (2020)

ENVIRONMENTAL IMPACT OF DIGITAL TECHNOLOGIES



5 Critical Materials for Digital

	49 In	INDIUM <i>Displays (touch screen)</i>
Chinese BAN 	31 Ga	GALLIUM <i>Semiconductors (smartphones, laptops...)</i>
	73 Ta	TANTALE <i>Capacitance (videos, RF, Smartphone)</i>
	60 Nd	NEODYMIUM <i>Magnets (microphone)</i>
Chinese BAN 	32 Ge	GERMANIUM <i>Semiconductors, optical fiber and infrared imagers</i>



- ⊕ ⊕ Growth of uses
- ⊕ ⊕ ⊕ Water
- ⊕ Geopolitical tensions
and competition for energy
and resources

**Digital technologies
must reduce
their ecological
footprint**

A large pile of electronic waste (e-waste) is shown on the left and right sides of the image. The waste includes various electronic components, circuit boards, and what appears to be old computer monitors. In the background, a large plume of dark smoke or steam rises from the waste pile into a cloudy sky. The central part of the image is a solid red rectangle containing white text.

**As ecosystems and living
conditions decline,
and the demand for rare,
hard-to-recycle minerals
increases,
we must find alternatives.**

PERSPECTIVES

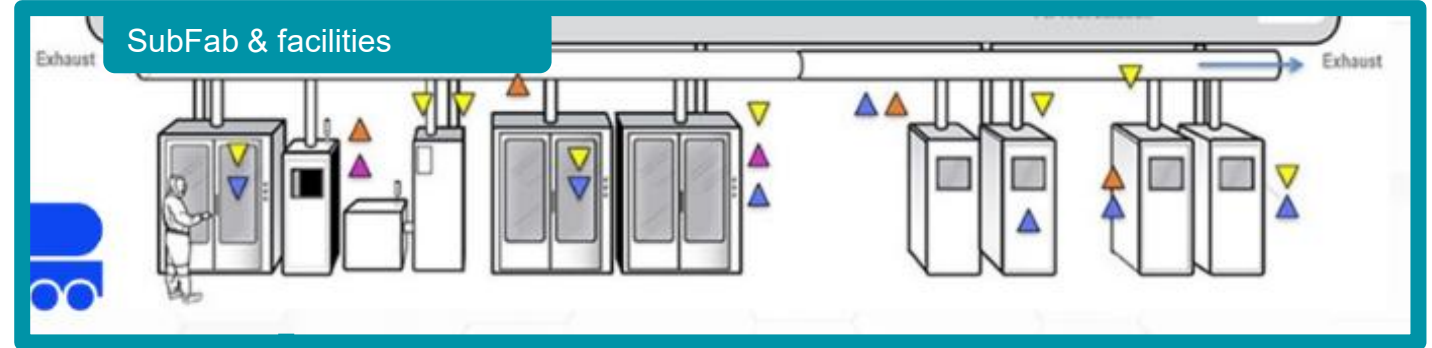
3

RESOLVE : Toward Energy-Efficient and Sustainable Electronics

TOWARDS SUSTAINABLE MANUFACTURING

CEA-LETI COORDINATES “GENESIS EU-PROJECT”

58 partners involved from 12 countries



GASES & CHEMICAL

- PFAS free materials (litho, bonding, eqpt)
- Low GWP gas (etch & clean)



PROCESS

- Technology sustainable alternatives (FEOL-BEOL – Packaging)
- Optimized use of rare earths, Ga, Ge...



WASTE MONITORING & TREATMENT

- By-products & wastes sensing & monitoring
- Filtration and adsorption solutions (PFAS...)
- Reuse



AIR EMISSIONS

- Reduce gas emissions
- Abatement
- H2 gas carrier re-use (MOCVD)



FINAL TREATMENT

- Reduce aqueous emission
- Water abatement
- Develop CRM recycling & valorization solutions

A NEW PARADIGM IS NEEDED TO FAVOR SOBRIETY/FRUGALITY VS. DECLINISM...



SPEED+



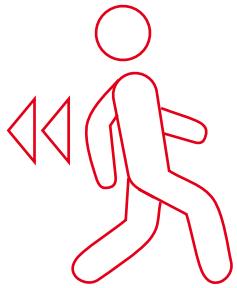
PERFORMANCE+



MINIATURIZATION



COST REDUCTION



DECLINISM

Pessimist's approach

Reducing or limiting performance

SOBRIETY

Athlete's approach

Maximizing performance with given resources



...and drastically reduce the energy
and environmental footprint of electronic devices



R.E.S.O.L.V.E
GREENER CHIPS

2025

2030

2032

ENERGY
EFFICIENCY
GAIN
× 1,000
by 2032

**The Challenge: Capitalize on
hardware and software advances
to master global digitization
and preserve the planet**



If you share
the same vision,
Join us!

jean-rene.lequepeys@cea.fr



R.E.S.O.L.V.E